AMENDMENTS TO THE CLAIMS

This listing of the claims will replace all prior versions, and listings, of claims in the application:

1-15.   (Canceled)

16. (New) An endian transformation method to enable program code of a first endian format to run on hardware of a different second endian format, wherein the hardware includes at least a processor and a memory, the method comprising the computer-implemented steps of:

      (a)   in a translation phase:

allocating a memory address range in the memory of length A bytes comprising a plurality of words arranged in a first relative order with respect to a starting address S;

receiving a plurality of input code instructions having memory access addresses which address the memory address range according to the first endian format for ordering the significance of bytes within words, where each access address B is of a respective string length L;

transforming each of said memory access addresses into transformed address expressions according to the expression A B L+S; and

translating the plurality of input code instructions into output code instructions executable by the hardware of the different endian format, where said output code instructions include said transformed address expressions; and

      (b)   in an execution phase:

executing said output code instructions on said hardware to fetch and store data in the memory in the allocated memory address range using the transformed address expressions, whereby the relative order of bytes within each word is reversed into the second endian format and the plurality of words are addressed in a second relative order with respect to the given starting address which is a reverse of the first relative order.

17. (New) The method of claim 16, further comprising the steps of:

in the translation phase:

identifying one or more constant terms and one or more variable terms in the expression A-B-L+S; and

providing partially resolved transformed address expressions in the translated output code instructions, where the partially resolved transformed address expressions include the one or more variable terms and group together the one or more constant terms in the expression A-B-L+S; and

in the execution phase:

completing calculation of the expression A-B-L+S for each of the partially realised transformed address expressions according to the one or more variable terms to provide fully resolved transformed memory access addresses; and

in said executing step, executing said output code instructions on said hardware of the different endian format to fetch and store data in the memory using the fully resolved transformed memory access addresses.

18. (New) The method of claim 16, wherein the program code is written for a big-endian architecture and the hardware has a little-endian architecture, or vice versa.

19. (New) An emulation system arranged to execute program code of a first endian format on hardware of a different second endian format, the emulation system comprising:

a processor;

a memory coupled to the processor;

a translator arranged to allocate a memory address range in the memory of length A bytes comprising a plurality of words arranged in a first relative order with respect to a starting address S, receive a plurality of input code instructions having memory access addresses which address the memory address range according to the first endian format for ordering the significance of bytes within words, where each access address B is of string length L, transform each of said memory access addresses into transformed address expressions according to the equation A B L+S, and translate the plurality of input code instructions into output code instructions executable by the hardware of the different second endian format, where said output code instructions include said transformed address expressions; and

wherein the processor is arranged to execute said output code instructions to fetch and store data in the memory in the memory address range using the transformed address

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expressions, whereby the relative order of bytes within each word is reversed into the second endian format and the plurality of words are addressed in a second relative order with respect to the given starting address which is a reverse of the first relative order.

20. (New) The emulation system of claim 19, wherein:

the translator is arranged to identify one or more constant terms and one or more variable terms in the expression A-B-L+S and provide partially resolved transformed address expressions in the translated output code instructions, where the partially resolved transformed address expressions include the one or more variable terms and group together the one or more constant terms in the expression A-B-L+S; and

the processor is arranged to execute said output code instructions including completing calculation of the expression A-B-L+S for each of the partially realised transformed address expressions according to the one or more variable terms to provide fully resolved transformed memory access addresses and to fetch and store data in the memory using the fully resolved transformed memory access addresses.

21. (New) The emulation system of claim 19, wherein the program code is written for a big-endian architecture and the hardware has a little-endian architecture, or vice versa.